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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/550,598	07/24/2006	Hee-Seob Kim	PNK-0228	1402
23413	7590	08/26/2009	EXAMINER	
CANTOR COLBURN, LLP 20 Church Street 22nd Floor Hartford, CT 06103			CALEY, MICHAEL H	
			ART UNIT	PAPER NUMBER
			2871	
			NOTIFICATION DATE	DELIVERY MODE
			08/26/2009	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

usptopatentmail@cantorcolburn.com

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/550,598	KIM ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Michael H. Caley	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 09 July 2009.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-14 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-4,6-9 and 11-14 is/are rejected.  
 7) Claim(s) 5 and 10 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 23 September 2005 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____.	6) <input type="checkbox"/> Other: _____ .

**DETAILED ACTION**

***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/9/09 has been entered.

***Specification***

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested:

Liquid crystal display having particular coupling between pixel electrodes and panel  
therefor

***Claim Objections***

Claims 7 and 13 are objected to because of the following informalities:

Regarding claim 7, line 6, "contract" should be "contact"

Regarding claim 13, "a first domain partitioning member" is introduced twice in lines 3 and 5.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**Claims 1-4, 6-9, and 11-14 are rejected under 35 U.S.C. 102(e) as being anticipated**

**by Song (U.S. Patent No. 7,460,191).**

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1 and 8, Song discloses a thin film transistor array panel comprising:

an insulating substrate (Figures 9-11 element 10);

a plurality of gate lines (20) formed on the insulating substrate;

a plurality of storage electrode lines (30) formed on the first insulating substrate

and including a storage electrode (portion forming csta, cstb);

a plurality of data lines (70) insulated from the gate lines and intersecting the gate lines; and

a plurality of groups, each group comprising:

a pair of first and second pixel electrodes (e.g. 92, 91) capacitively coupled to each other (Figure 12), disposed on pixel areas defined by intersections of the gate lines and the data lines and arranged in a matrix;

a first thin film transistor (having drain 73) connected to one of the gate lines and one of the data lines, and connected to the first pixel electrode;

a second thin film transistor (having drain 72, below first transistor) connected to or capacitively coupled to the second pixel electrode; and

a coupling electrode (74) connected to one of the first pixel electrode and the second pixel electrode and overlapping the other of the first pixel electrode and the second pixel electrode, wherein the coupling electrode partially overlaps the storage electrode (Figure 9).

Regarding claim 2, Song discloses the storage electrode and the coupling electrode as overlapping an edge of one of the first and second pixel electrodes (Figure 9).

Regarding claims 3, 9, and 11, Song discloses the coupling electrode as connected to a drain electrode of one of the first thin film transistor and the second thin film transistor (Figure 9).

Regarding claim 4, Song discloses the second thin film transistor as connected to one of the storage electrode lines and the data lines (Figure 9).

Regarding claims 6 and 13, Song discloses the first and second domain partitioning member (91, 92, 510).

Regarding claims 7 and 12, Song discloses a gate insulating layer (40) disposed between the gate lines and the data lines; and a passivation layer (80) disposed between the data lines and the first and the second pixel electrodes, wherein the coupling electrode is connected to the first pixel electrode through a contact hole at the passivation layer (Figure 11).

**Claims 1-4, 6, 8, 9, 11, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Hiraishi (U.S. Patent No. 6,104,450).**

Regarding claims 1 and 8, Hiraishi discloses a thin film transistor array panel comprising:  
an insulating substrate (Figures 16 and 17 element 101a);  
a plurality of gate lines (102b) formed on the insulating substrate;  
a plurality of storage electrode lines (104) formed on the first insulating substrate and including a storage electrode (portion beneath 112, 114).;  
a plurality of data lines (103) insulated from the gate lines and intersecting the gate lines; and  
a plurality of groups, each group comprising:

a pair of first and second pixel electrodes (112, 114) capacitively coupled to each other (Figure 3), disposed on pixel areas defined by intersections of the gate lines and the data lines and arranged in a matrix;

a first thin film transistor (105a) connected to one of the gate lines and one of the data lines, and connected to the first pixel electrode;

a second thin film transistor (105b) connected to or capacitively coupled to the second pixel electrode; and

a coupling electrode (portion of 114 overlapping 104) connected to one of the first pixel electrode and the second pixel electrode and overlapping the other of the first pixel electrode and the second pixel electrode, wherein the coupling electrode partially overlaps the storage electrode (Figure 9).

Regarding claim 2, Hiraishi discloses the storage electrode and the coupling electrode as overlapping an edge of one of the first and second pixel electrodes (Figure 16).

Regarding claims 3, 9, and 11, Hiraishi discloses the coupling electrode as connected to a drain electrode of one of the first thin film transistor and the second thin film transistor (Figure 16).

Regarding claim 4, Hiraishi discloses the second thin film transistor as connected to one of the storage electrode lines and the data lines (Figure 16).

Regarding claims 6 and 13, Hiraishi discloses the first and second domain partitioning member (114a).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Song in view of Mimura et al. (U.S. Patent No. 5,283,566 “Mimura”).**

Song fails to disclose two storage lines as connected to each other through a storage bridge. Mimura, however, teaches a storage bridge (Figure 1 element 9) for maintaining the storage electrode at a same fixed potential (Column 3 lines 12-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a storage bridge connecting storage electrode lines as proposed. One would have been motivated to form the storage bridge as a means of maintaining the fixed potential among storage lines to maximize the storage capacitance function according to conventional means (Mimura: Column 3 lines 12-16).

**Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiraishi in view of Mimura.**

Hiraishi fails to disclose two storage lines as connected to each other through a storage bridge. Mimura, however, teaches a storage bridge (Figure 1 element 9) for maintaining the storage electrode at a same fixed potential (Column 3 lines 12-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a storage bridge connecting storage electrode lines as proposed. One would have been motivated to form the storage bridge as a means of maintaining the fixed potential among storage lines to maximize the storage capacitance function according to conventional means (Mimura: Column 3 lines 12-16).

*Allowable Subject Matter*

**The indicated allowability of claims 8-13 is withdrawn in view of the newly discovered reference(s) to Song and Hiraishi.**

**Claims 5 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.**

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to disclose or suggest the particular configuration in which the second thin film transistor is connected to one of the storage electrode lines and the third thin film transistor connected as proposed.

***Response to Arguments***

Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael H. Caley whose telephone number is (571)272-2286. The examiner can normally be reached on M-F 6:00 a.m - 2:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael H. Caley/  
Primary Examiner, Art Unit 2871